Application No. 10/077,730   Docket No.: 83180US1
Amendment dated September 30, 2005
Reply to Office Action of June 1, 2005

AMENDMENTS TO THE ABSTRACT

Please substitute the following paragraph for the abstract now appearing in the currently filed specification:

An automatic gain control RF signal processor for receiver systems includes an attenuator, an amplifier, a bandpass filter, a single analog to digital converter (ADC), a digital logic circuit, and a first in first out (FIFO) buffer. The digital logic circuit includes signal detection logic for detecting the presence of a pulse within the ADC signal, determining a peak amplitude value of the pulse, and generating an attenuation value applied to the variable gain control input of the attenuator. The sampling logic averages a number of ADC data samples to determine a moving average pulse amplitude, and compares this moving average pulse amplitude to a processing threshold value to determine a delta value with which to adjust the attenuation value and to determine when to terminate a pulse and reset the attenuation value to zero. The averaging determines whether the pulse should be terminated.